REMARKS

Applicant thanks the Examiner for acknowledging Applicant's claim to foreign priority, and for indicating that the certified copy of the priority document, Japanese Patent Application No. Hei 11-234811 dated August 20, 1999, has been made of record in the file.

The Examiner objects to the Drawings as filed. Applicant is concurrently filing a Request for Approval of Proposed Drawing Corrections with this Amendment.

Applicant herein amends the written description of the instant application. The amendments are editorial in nature, and add no new matter.

Applicant herein amends claims 1 and 2 to remove typographical error. The amendments do not narrow the literal scope of claims 1 and 2, and are not made for any reasons of patentability. Entry and consideration of the amendments to claims 1 and 2 is respectfully requested.

Claim 5 has been amended to more properly claim the invention. Entry and consideration of the amendments to claim 5 is respectfully requested.

Claims 1-19 are all the claims presently pending in the application.

1. Claims 12 and 13 stand rejected under 35 U.S.C. § 112, first paragraph as containing subject matter not described in the specification. Applicant herein amends claims 12 and 13 to recite mode definitely that the source and gate of the MOSFET are connected to the ground wire. The amendment to claims 12 and 13 does not narrow the literal scope of claims 12 and 13 in any manner. Applicant respectfully requests that the Examiner withdraw the § 112 rejection.

2. Claims 16 and 19 are withdrawn from consideration pursuant to 37 C.F.R. § 1.142(b) as being drawn to non-elected embodiments.

With regard to claim 16, which depends from claim 1, the written description clearly states that for the embodiment of Figure 1, the electrostatic protection element 18 can be a field effect transistor, a bipolar transistor, a thyrister or a diode. See page 18, lines 3-6 of the written description of the instant application. Applicant respectfully requests that claim 16 be rejoined and examined.

With regard to claim 19, Applicant's Response to Election of Species Requirement contained a typographical error as claim 18 should have been elected for examination. Support for claim 18, which depends from claim 1, is found on page 18, lines 3-6 of the written description of the instant application. Applicant respectfully requests that the Examiner consider claim 18.

3. Claims 1, 3, 8, 10, 12 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozaki et al. (U.S. Patent No. 4,456,939) in view of Miller (U.S. Patent No. 5,255,146). Applicant respectfully traverses the rejection of claims 1, 3, 8, 10, 12 and 13.

Ozaki et al. discloses, *inter alia*, a MIS transistor used as an input protective circuit for a semiconductor device. In Fig. 2 of Ozaki et al., a MIS transistor 108 is connected to an input to a semiconductor device 102, wherein the source and gate electrodes of the MIS transistor 108 are connected to the ground potential, and the drain electrode of the MIS transistor 108 is connected to the input of the semiconductor device 102. See, col. 2, lines 55-61 of Ozaki et al. In addition,

the electrostatic gate capacitance of the MIS transistor 101 is shown as equivalent circuit 106. See, col. 2, lines 52-55 of Ozaki et al.

The Examiner acknowledges that Ozaki et al. fails to teach or suggest that the wire resistance of the ground potential wire between the ESD element connection point and the ground terminal is larger that the wire resistance of the ground potential wire between the ESD element connection point and the MOS capacitor connection point. To overcome the deficiencies of Ozaki et al., the Examiner states that the positioning of the ESD element connection point on the ground potential wire relative to the MOS capacitor connection point on the ground potential wire would be a matter of design choice within the skills of an artisan. The Examiner also takes "judicial notice" of the computer-aided design of the layout of integrated circuits.

Applicant respectfully reminds the Examiner that he can only take official notice of well-known facts in accord with MPEP § 2144.03, not "judicial notice." Applicant respectfully traverses the Examiner's official notice regarding computer-aided design of integrated circuits, as the Examiner has not cited any reference which teaches or suggests the positioning of an electrostatic protection element with respect to an MOS capacitor, such that the ground wire resistance between the electrostatic protection element and ground terminal connection points is larger than the ground wire resistance between the electrostatic protection element and MOS capacitor connection points, as recited in claim 1.

Furthermore, the Examiner appears to be ignoring the recitations of claim 1, as Ozaki et al. lacks any teaching or suggestion of connecting a MOS capacitor in parallel with an

electrostatic protection element between a power source wire and a ground potential wire, as recited in claim 1. Moreover, the circuit illustrated in Fig. 2 of Ozaki et al. is identical to the circuit shown in Fig. 17 of the instant application. The "MIS capacitor" of Ozaki et al. (i.e., the gate capacitance of MIS transistor 101) is connected between a signal input and a ground potential, not between a power source line and ground potential wire.

In addition, Applicant does not agree with the Examiner's bald assertion that it is merely a matter of design choice for the placement of the electrostatic protection element with respect to the MOS capacitor. The Examiner has acknowledged that Ozaki et al. fails to teach or suggest the ground wire resistance relationship, and the Examiner has failed to cite any computer-aided design reference that describes the ground wire resistance relationship. In order to protect the MOS capacitor, the wire resistance of the ground potential wire must be taken into consideration. See, page 18, line 20 to page 20, line 5 of the written description of the instant application.

In the alternative, the Examiner combines Ozaki et al. with Miller in order to overcome the acknowledged deficiencies of Ozaki et al. The combination of Ozaki et al. and Miller, however, fails to teach or suggest the invention recited in claim 1. The Examiner cites Miller as teaching the placement of a electrostatic protection element with respect to a ground terminal and a MOS capacitor, such that the ground wire resistance between the ground terminal and electrostatic protection element connections is greater than the ground wire resistance between the electrostatic protection element and MOS capacitor connections. In Fig. 2 of Miller, however, there is no indication that the ESD protection circuit 14 is positioned relative to a MOS capacitor such that the resistive relationship as claimed in claim 1 is taught or suggested. Thus,

Applicant believes that claim 1 is allowable over the combination of Ozaki et al. and Miller, and Applicant further believes that claims 3, 8, 10, 12 and 13 are allowable, at least by virtue of their dependency from claim 1.

Since claim 1 is generic to claim 2-19, Applicant respectfully requests that claims 2, 4-7, 9, 11, 14, 15, 17 and 18 be reinstated under 37 C.F.R. § 1.142(b) and indicated as allowable as well.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Please charge any fees necessary to maintain the pendency of this application, except for the Issue Fee, to our Deposit Account No. 19-4880.

Respectfully submitted,

Paul J. Wilson
Registration No. 45,879

SUGHRUE, MION, ZINN,
MACPEAK & SEAS, PLLC
2100 Pennsylvania Avenue, N.W.
Washington, D.C. 20037-3213
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

Date: July 3, 2001

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification is changed as follows:

Page 8, first full paragraph:

Thus, since the above described conventional techniques (Japanese Examined Patent Application, Second Publication No. Hei 7-24310, Japanese Patent (Granted) Publication No. 2650276, and Japanese Unexamined Patent Application, First Publication No. Hei 7-183457) do not relate to the CDM which is the breakdown model of the semiconductor integrated circuit of the present invention, the discharge path in the semiconductor integrated circuit of the present invention during electrostatic breakdown differs from those of the conventional integrated circuits. In addition, in contrast to the present application, which used the MOS capacitor provided between the power source wire and the ground potential wire as the element subjected to protection against electrostatic breakdown, the conventional techniques make use of the gate of the MOS [MOD] transistor located in between the input/output terminals and the ground potential wire.

Page 19, first full paragraph:

When the discharge test switch 2 is turned on after the semiconductor integrated circuit device according to the first embodiment is subjected to electrification, the charge charged in the capacitance held by the ground potential wire 12 from the ground terminal 14 [15] is discharged to the ground. At this time, the voltage between both terminals of the MOS capacitor is clamped

at a voltage lower than the dielectric breakdown voltage by the electrostatic [dielectric] protection element 18. Thus, the MOS capacitor is protected from the electrostatic breakdown.

IN THE CLAIMS:

The claims are amended as follows:

1. (*Amended*) A semiconductor integrated circuit device comprising:

a MOS capacitor, one end of which is connected to a power source wire for supplying a power source voltage, and another end of which is connected to a ground potential wire for supplying a ground potential;

a ground terminal, to which said ground potential wire is connected; and

an electrostatic protection element connected in parallel with said MOS capacitor between said ground terminal and said MOS capacitor;

wherein, a wire resistance of said ground potential wire between a connection point on said ground wire with one end of said electrostatic protection element and said ground terminal is larger than a wire resistance of said ground potential wire between said connection point on said ground potential wire with one end of said electrostatic protection element and a connection point on said ground potential wire with the other end of said MOS capacitor.

2. (*Amended*) A semiconductor integrated circuit device comprising:

an electrostatic protection element, one end of which is connected to a power source wire for supplying a power source voltage, and another end of which is connected to a ground potential wire for supplying a ground potential;

a ground terminal, to which said ground potential wire is connected; and

a MOS capacitor connected in parallel with said electrostatic protection element between said ground terminal and said electrostatic protection element;

wherein, a wire resistance of said ground potential wire between a connection point on said ground wire with one end of said MOS capacitor and said ground terminal is larger than a wire resistance of the ground potential wire between said connection point on said ground potential wire with one end of said MOS capacitor and a connection point on said ground potential wire with the other end of said electrostatic protection element.

5. (*Amended*) A semiconductor integrated circuit device comprising:

an input/output terminal;

a first electrostatic protection element, one end of which is connected to said input/output terminal and another end of which is connected to a ground potential wire for supplying the ground potential;

a second electrostatic protection element, one end of which is connected to a power source wire for supplying a power source voltage, [one end of which is connected to said input/output terminal] and another end of which is connected to a ground potential wire for supplying the ground potential; and

a MOS capacitor connected in parallel with said second electrostatic protection element between said first electrostatic protection element and said second electrostatic protection element;

wherein a wire resistance of the ground potential wire between the connection point on the ground potential wire with the other end of said first electrostatic protection element and the connection point on the ground potential wire with one end of said MOS capacitor is larger than a wire resistance of the ground potential wire between the connection point on the ground potential wire with the one end of said MOS capacitor and the connection point on the ground potential wire with the other end of said second electrostatic protection element.

12. (*Amended*) A semiconductor integrated circuit device according to any one of claims 1 and 2, wherein said electrostatic protection element is a MOS field effect transistor, the drain of which is connected to said power source wire, and the source and the gate [drain] of which are connected to said ground potential wire.

13. (*Amended*) A semiconductor integrated circuit device according to any one of claims 4 and 5, wherein said second electrostatic protection element is a MOS field effect transistor, the drain of which is connected to said power source wire, and the source and the gate [drain] of which are connected to said ground potential wire.